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Reduced Test Pattern Generation of Multiple SIC Vectors with Input and Output Delay Faults

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ABSTRACT
In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. Most of the methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation [1]. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation [1]–[3]. In the proposed pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power. In VLSI testing, power reduction is achieved by increasing the correlation between consecutive test patterns.

Keywords **-** Built in Self Test (BIST) , Johnson ring counter, MSIC patterns, Test Pattern Generator (TPG), Circuit Under Test (CUT).

I. INTRODUCTION

A fault is a representation of a defect reflecting a physical condition that causes a circuit to fail to perform in a required manner. To test a circuit with n inputs and m outputs, a set of input patterns is applied to the circuit under test (CUT), and its responses are compared to the known good responses of a fault-free circuit. Each input pattern is called a test vector. In order to completely test a circuit, many test patterns are required; however, it is difficult to know how many test vectors are needed to guarantee a satisfactory reject rate. If the CUT is an n-input combinational logic circuit, we can apply all 2^n possible input patterns for testing stuck-at faults; this approach is called exhaustive testing. Unfortunately, exhaustive testing is not practical when n is large. BUILT-IN SELF-TEST (BIST) techniques can effectively reduce the difficulty and complexity of VLSI testing, by introducing on-chip test hardware into the circuit-under-test (CUT). In conservative BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. A major disadvantage of these architectures is that the pseudorandom patterns generated by the LFSR provide to considerably high switching behavior in the CUT [1], which can cause too much power dissipation. They can also spoil the circuit and decrease product yield and life span [2], [3]. In addition, the LFSR usually needs to generate very lengthy pseudorandom sequences in order to attain the target fault coverage in nanometer technology.

II. PRELIMINARIES

A. Prior Work

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard *et al.* analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4]. The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno *et al.* provided a low power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in [7] reduces the power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent. However, this dependency implies that non detecting subsequences must be determined for each circuit test sequence. Bonhomme *et al.* [9] used a clock gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia *et al.* [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to

logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [13]–[15]. These architectures apply the minimum number of test vectors required to attain the target fault coverage and therefore reduce the power. However, these methods have high area overhead, need to be customized for the CUT, and start with a specific seed. Gerstendorfer *et al.* also proposed to filter out non detecting patterns using gate-based blocking logics [16], which, however, add significant delay in the signal propagation path from the scan flip-flop to logic. Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan enable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR [20], a low-transition random TPG [21], and the weighted LFSR [22]. The TPG in [20] can reduce the transitions in the scan inputs by assigning the same value to most neighboring bits in the scan chain. In [21], power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in [22] decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various probabilities.

B. Contribution and Paper Organization

This paper presents the theory and application of a class of minimum transition sequences. The proposed method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence can be summarized as follows.

1) *Minimum transitions:* In the proposed pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power.

2) *Uniqueness of patterns:* The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT.

3) *Uniform distribution of patterns:* The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time [23]. It is proved in this paper that our multiple SIC (MSIC) sequence is nearly uniformly distributed.

4) *Low hardware overhead consumed by extra TPGs:* The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential decompressor. Hence, the proposed TPG can be easily implemented by hardware.

The rest of this paper is organized as follows. In Section III, the proposed MSIC-TPG scheme is presented. The Properties of the new MSIC sequences is described in Section IV. In Section V, Implementation of MSIC TPG In BIST Architecture is analyzed. The Section VI and VII explains, Performance analysis, experimental results on test vectors and Transition density the performance of the proposed MSIC-TPGs. Conclusions are given in Section VIII.

III. METHODOLOGY

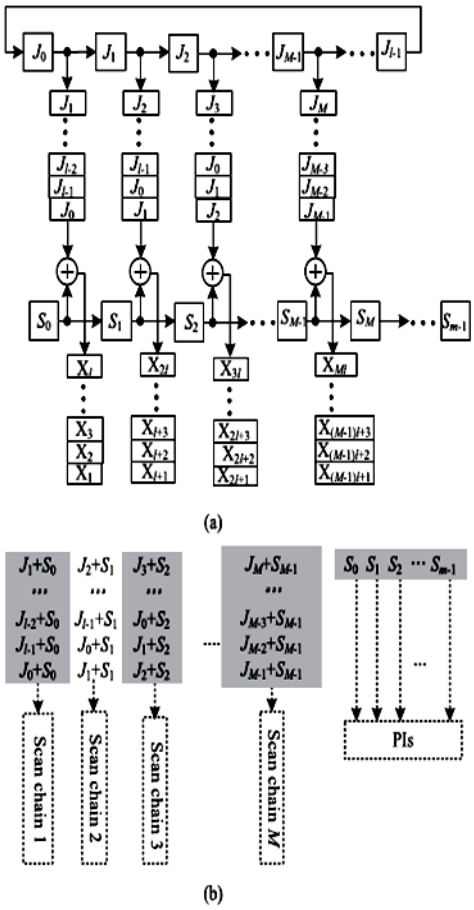


Fig. 1. (a) Symbolic simulation of an MSIC pattern for scan cl
(b) Symbolic representation of an MSIC pattern.

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple codewords. Meanwhile, the generated codewords will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

A.Test Pattern Generation Method

Assume there are *m* primary inputs (PIs) and *M* scan chains in a full scan design, and each scan chain has *l* scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an *m*-bit LFSR with the primitive polynomial can be expressed as $S(t) = S0(t)S1(t)S2(t), \ldots, Sm-1(t)$ (hereinafter referred to as the seed), and the vector generated by an *l*-bit Johnson counter can be expressed as $J(t) = J0(t)J1(t)J2(t), \ldots, Jl-1(t)$. In the first clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will bit-XOR with $S = S0S1S2, \ldots, SM-1$, and the results $X1Xl+1X2l+1, \ldots, X(M-1)l+1$ will be shifted into *M* scan chains, respectively. In the second clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will be circularly shifted as $J = Jl-1\ J0\ J1, \ldots, Jl-2$, which will also bit-XOR with the seed $S = S0S1S2, \ldots, SM-1$. The resulting $X2Xl+2X2l+2, \ldots, X(M-1)l+2$ will be shifted into *M* scan chains, respectively. After *l* clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S0S1S2, \ldots, Sm-1$ will be applied to *m* PIs. Since the circular Johnson counter can generate *l* unique Johnson codewords through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential decompressor.

B. Reconfigurable Johnson Counter

According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson codewords, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

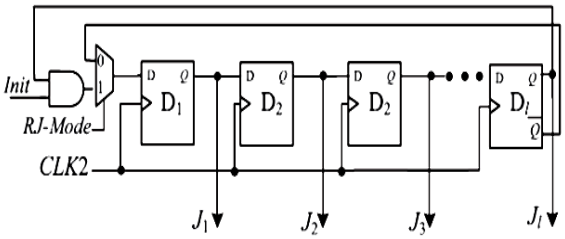


Fig. 2. Reconfigurable Johnson counter.

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 2(a), it can operate in three modes.

1) *Initialization:* When RJ_Mode is set to 1 and *Init* is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than *l* times.

2) *Circular shift register mode:* When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK 2*l* times.

3) *Normal mode:* **When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2*l* unique SIC vectors by clocking CLK2 2*l* times.**

The applied vectors will generate SIC vectors by using the below architectural description, it is a rotational shift register which will rotated sequences based on input values

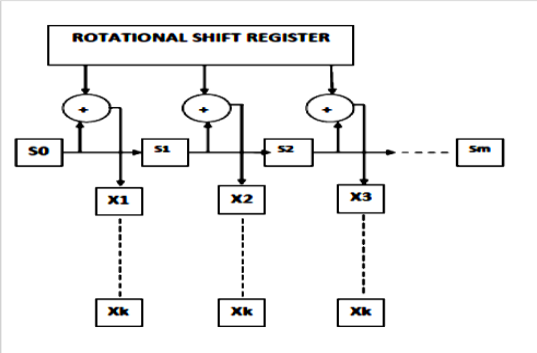


Fig4. Rotational shift register

The last bit of the generated sequence is applied as input to the next register and every bit of the generated sequence is XORed with with its seed value. Seed is a initial value it can be any random vector the generated SIC sequence depends upon the applied seed also as the no of changes in seed increases the output Single input change vectors also increases.

C. MSIC-TPGs for Test-per-Scan Schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 5(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to *M* scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

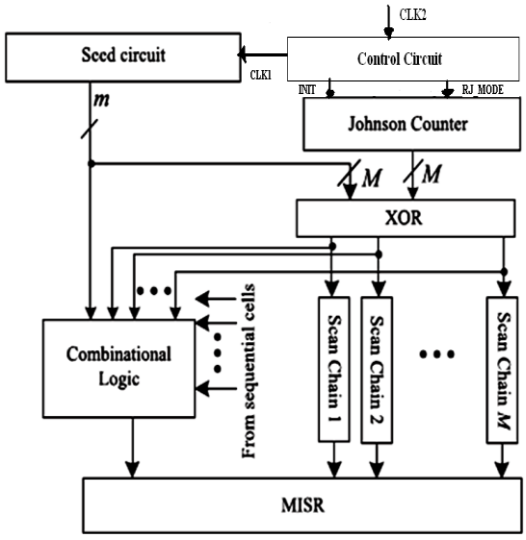
1) The seed circuit generates a new seed by clocking CLK1 one time.

2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.

3) After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates *l* codewords by clocking CLK2 *l* times. Then, a capture operation is inserted.

4) Repeat 2–3 until 2*l* Johnson vectors are generated.

5) Repeat 1–4 until the expected fault coverage or test length is achieved.



Fig;5(b) MSIC-TPG Test per Scan Scheme

IV. PROPERTIES OF MSIC SEQUENCES

A. Switching Activity Reduction

For test-per-clock schemes, *M* segments of the CUT's primary inputs are applied with *M* unique SIC vectors. The mean input transition density of the CUT is close to 1/*l*. For test-per-scan schemes, the CUT's PIs are kept unchanged during 2*l*2 shifting-in clock cycles, and the transitions of a Johnson codeword are not greater than 2. Therefore, the mean input transition density of the CUT during scan-in operations is less than 2/*l*.

B. Uniform Distribution of MSIC Patterns

If test patterns are not uniformly distributed, there might be some inputs that are assigned the same values in most test patterns. Hence, faults that can only be detected by patterns that are not generated may escape, leading to low fault coverage.

C. Relationship between Test Length and Fault Coverage

The test length of conventional LFSR methods is related to the initial test vector. In other words, the number of patterns to hit the target fault coverage depends on the initial vector in conventional LFSR TPGs. For MSIC sequences, the numbers of patterns to hit the target fault coverage with different initial seeds are nearly the same, as shown by curves marked with "Best case, MSIC" and "Worst case, MSIC." Also, the rate of growth of the fault coverage with the MSIC sequence is very close to that with the LFSR in the best case.

V. IMPLEMENTATION OF MSIC TPG IN BIST ARCHITECTURE

The MSIC TPG which generates MSIC vectors i.e., patterns that should be given as input to the CUT as well as the reference circuit. The patterns

should be unique and uniformly distributed among them. The circuit which intakes the vectors of TPG it generates the output responses and that responses are equal to the reference circuit output responses. The resultant of both responses gets compared to each other at comparator circuit i.e., Test Response Analyzer (TRA) and delivers the result. Like this, the testing of CUT'S are easily done with the help Of TPG'S.One more factor MISR'S plays a major role in the BIST ARCHITECTURE which stores the output responses of CUT and Reference Circuit. A typical BIST architecture which is shown in fig (4) consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit. SIC technique is a low power approach which greatly decreases the transitions of inputs to reduce the internal switching activities. In SIC the number of bits in sequence will change only one but we need more vectors requires to test CUT, which needs more time for testing. MSIC has multiple chain vectors, each chain will change one bit we need minimum number of vectors requires in the CUT testing, by using this method we can improve the power dissipation, speed, yield and life time.

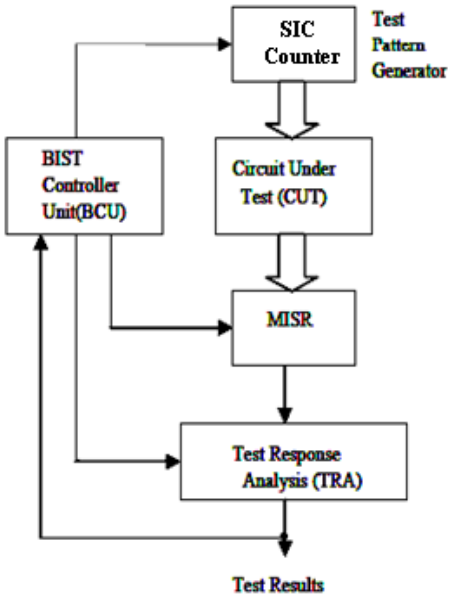


Fig6. MSIC TPG in BIST Architecture

The blocks of BIST ARCHITECTURE is explain as follows:

□ □ TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

□ □ MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures.

□ □ TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

□ □ BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

□ □ CUT: It is the portion ofthe circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.

VI. PERFORMANCE ANALYSIS

The performance simulations of MSIC TPG along with CUT testing are carried out with MODELSIM ALTERA 6.5e Simulator. Synthesis has been carried out with XILINK ISE. The test frequency is 14.96 MHz, the power supply voltage is 1.1 V and delay of 66.82ns.The number of multiplier required is 1, registers and flip flops are 104, comparators 1,exor gates 993 and the number of IO's is 13. The CUT 32 bit array multiplier is successfully been tested by MSIC TPG of BIST Architecture. Whereas with LFSR TPG the accurate testing of CUT will not be occur because of high switching activities.

VII. EXPERIMENTAL RESULTS

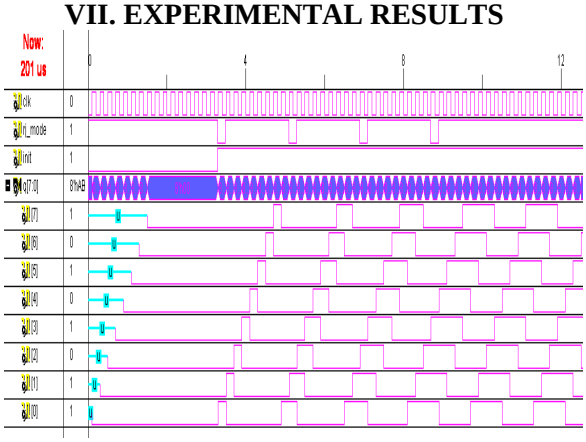


Fig 6. Johnson Counter Simulation Results

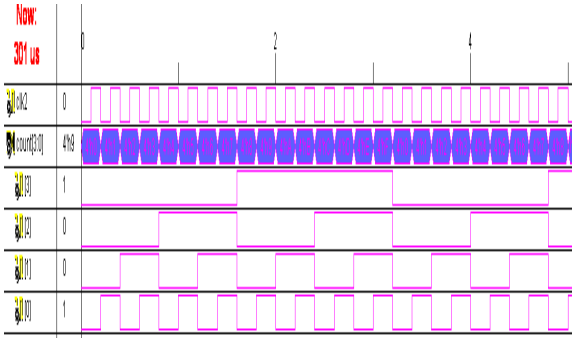


Fig 7. Seed Generator Simulation Results

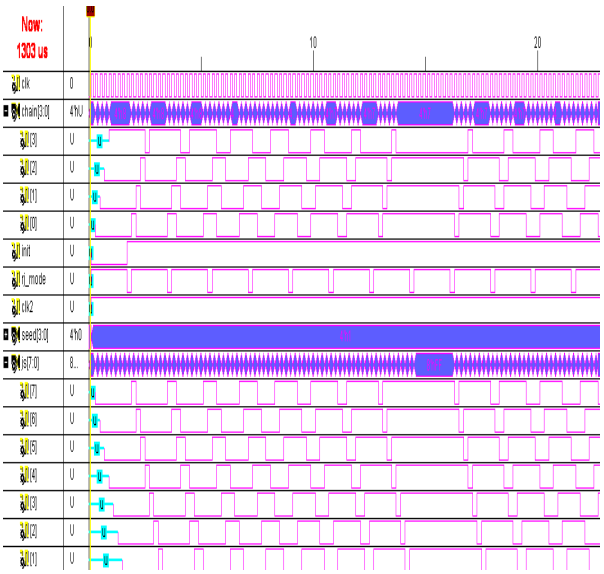


Fig 8. MSIC TPG Patterns

VIII. CONCLUSION

This paper has proposed a low-power test pattern generation method that could be easily implemented by hardware. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SIC sequences named MSIC. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. For a test-per-clock scheme, the MSIC-TPG applies SIC sequences to the CUT with the SRAM-like grid. For a test-per scan scheme, the MSIC-TPG converts an SIC vector to low transition vectors for all scan chains. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead.

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